

## REMARKS

The Office Action dated January 18, 2005, has been received and carefully noted.

The following remarks are submitted as a full and complete response thereto.

Claims 1, 3, 5, 9 and 13 are amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter is added and no further consideration and/or search is required. Thus, claims 1-15 are pending in the subject application and are respectfully submitted for consideration.

Claims 1-15 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,760,341 (*Erimli et al.*). The Office Action took the position that *Erimli* taught each and every element of the claims. Applicants respectfully traverse the anticipation rejection and submit that the cited reference does not disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2-4 are dependent, recites a network of switches. The network includes a first switch having a first memory interface and a first expansion port. The network also includes a first memory coupled to the first switch with a first memory bus. The network also includes an expansion bus having a first expansion bus interface and a second expansion bus interface. The first expansion bus interface is connected to the first expansion port. The network of switches also includes a second switch having a second memory interface and a second expansion port. The second expansion port is connected to the second expansion bus interface, thereby connecting the first switch to the second switch. The network also includes a second memory coupled to the second

switch with a second memory bus. The expansion bus allows the first switch to directly access the second memory interface through the second switch and the second switch to directly access the first memory interface through the first switch to increase a bandwidth of a read/write operation to the first memory and the second memory..

Claim 5, upon which claims 6-8 are dependent, recites a switch for transmitting and receiving data packets. The switch includes a memory interface that accesses memory via a memory bus. The switch also includes an expansion port connected to the memory interface. The expansion port is configured to be connected to an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read/write operation.

Claim 9, upon which claims 10-12 are dependent, recites a system of network switches. The system includes a first switch having a first memory and a first expansion port. The system also includes an expansion bus having a first expansion bus end and a second expansion bus end. The first expansion bus end is connected to the first expansion port. The system also includes a second switch having a second memory and a second expansion port. The second expansion port is connected to the second expansion bus end, thereby connecting the first switch to the second switch. The expansion bus allows the first switch to directly access the second memory through the second switch and the second switch to directly access the first memory through the first switch to increase a bandwidth of a read/write operation to the first memory and the second memory.

Claim 13, upon which claims 14 and 15 are dependent, recites a method for sharing memory between a first switch and a second switch connected to each other by an expansion bus. The method includes sending a command from a first switch to a second switch that the first switch is about to perform a memory read or write. The method also includes reading or writing a portion of packet data to local memory of the first switch using a memory bus. The method also includes reading or writing another portion of packet data to alternate memory through the second switch using the expansion bus.

As discussed in the specification, examples of the present invention provide a switch having virtual shared memory. Examples of the present invention enable an expansion port to be provided on a switch to connect two switches together. Thus, two switches may read and write at a bandwidth of 128 Gbits/sec while maintaining a single memory bus master for each memory to reduce memory bus loading. Further, examples of the present invention may eliminate the need for two switches to be electrically connected to a centralized memory along a common bus. Thus, an electrical load may be decreased as compared to the use of a common bus. It is respectfully submitted that the cited reference fails to disclose or suggest all the elements of any of the presently pending claims. Therefore, the cited reference fails to provide the critical and unobvious advantages discussed above.

*Erimli* relates to the segmentation of buffer memories for shared frame data storage among multiple network switch modules. Each memory device is divided into memory segments, such that each memory segment is configured for storing frame data

from a corresponding one of the switch modules. Switching logic 28 of *Erimli* forwards a frame pointer specifying the location of the received data packet to the other multiport switches 22 via an expansion port 30. Each of switch modules 22 include a memory interface 44 configured for controlling the storage of frame data in buffer memory devices 36 according to a prescribed protocol. Referring to Figure 2 of *Erimli*, bus 32 connects the switch modules and buffer memory devices together. Memory interfaces 44 assign memory segment A in each of buffer memory devices 36 to switching module 22a, memory segment B in each of buffer memory devices 36 to switching module 22b, and memory segment C in each of the buffer memory devices 36 to switching module 22c. Thus, switch module 22a can write frame data only into memory segment A of buffer memory devices 36a, 36b and 36c and so on. Each memory interface 44 can use a single frame pointer that specifies a specific memory address location and read frame data for a stored data frame from memory devices 36.

Applicants submit that *Erimli* does not disclose or suggest all the features of the presently pending claims. For example, applicants submit that *Erimli* does not disclose or suggest “a first memory coupled to the first switch with a first memory bus,” “a second memory coupled to the second switch with a second memory bus,” and “said expansion bus allows said first switch to directly access said second memory interface through said second switch . . . to increase a bandwidth of a read/write operation to the first memory and the second memory,” as recited in claim 1. Further, applicants submit that the cited reference does not disclose or suggest “an expansion bus connected to another switch

thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read/write operation,” as recited in claim 5. Claim 9 recites the patentable features of claim 1, as well as other features, but is drawn to a system of network of switches. Moreover, applicants submit that the cited reference does not disclose or suggest “reading or writing a portion of packet data to local memory of said first switching using a memory bus” and “reading or writing another portion of packet data to alternate memory through said second switch using said expansion bus,” as recited in claim 13. Applicants respectfully submit that the cited reference does not disclose or suggest at least these features of the pending claims.

Applicants submit that *Erimli* does not disclose or suggest accessing two separate memories over an expansion bus and a memory bus. As shown in *Erimli*, bus 32 connects all the switch modules with each other and with the buffer memory devices. This aspect of *Erimli* does not disclose or suggest a first memory coupled to a first switch with a first memory bus, and a second memory coupled to a second switch with a second memory bus, and using an expansion bus to access the memories. By using two separate buses to perform, for example, a read/write operation, the bandwidth may be increased by the addition of the expansion bus in accessing the second memory. *Erimli* does not disclose or suggest this feature. Instead, *Erimli* describes, for example, a switch module 22a sending the data frame to its buffer memory device 36 and forwarding the rest of the packet to other switches without directly accessing the other memory devices or using an expansion bus. Thus, applicants submit that *Erimli* does not disclose or suggest at least

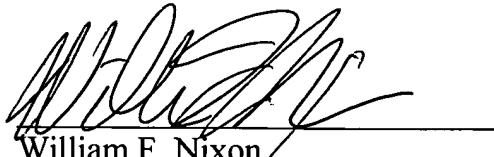
these features of the presently pending claims. Applicants respectfully request that the anticipation rejection be withdrawn.

It is submitted that each of claims 1-15 recites subject matter that is neither disclosed nor suggested by the cited reference. Therefore, it is respectfully requested that claims 1-15 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



\_\_\_\_\_  
William F. Nixon  
Registration No. 44,262

**Customer No. 32294**  
SQUIRE, SANDERS & DEMPSEY LLP  
14<sup>TH</sup> Floor  
8000 Towers Crescent Drive  
Tysons Corner, Virginia 22182-2700  
Telephone: 703-720-7800  
Fax: 703-720-7802

WFN:cct